# **CALIFORNIA STATE UNIVERSITY, NORTHRIDGE**

**Department of Electrical and Computer Engineering**

# **ECE 526L**

**LAB – 3: Delays for Primitives**

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**Introduction:**

In this lab, we learned about delays for primitive, firstly, we applied 0 ns delay then changes the delays as per the instructions from lab manuals.

**Methodology/Procedure:**

**Section 3\_1:**

1. Open a new folder as **Lab3\_526l**, create new file name as **Lab3\_1.v**
2. Write the code exactly as in the lab manual and set the initial delay as 0 ns for every delays.
3. Then, create another file name as **Lab3\_1\_tb.v**
4. Write the code as it was with all the possible combinations of the truth table.
5. After that, gave command **vcs -debug\_access+all Lab3\_1.v Lab\_3\_1.tb.v** to check the simulations and fix the errors.
6. Gave Command **simv**.
7. Create the log file as **Lab3\_1.Log** using **simv-l Lab3.log** and open **vcdplus.vpd**
8. Select all the signals and open DVE window.
9. Match the result with the truth table.

**Section 3\_2:**

1. Create a new file name as [**Lab3\_2.v**](mailto:Lab_3_@.v) **.**
2. Write the code exactly as in the lab manual and set the delay from the lab manual.
3. Then, create another file name as **Lab3\_2\_tb.v** , write the code as it was with all the possible combinations of the truth table.
4. After that, gave command **vcs -debug\_access+all Lab\_3\_2.v Lab\_3\_2.tb.v** to check the simulations and fix the error.
5. Gave Command **simv**.
6. Create the log file as **Lab\_3\_2.Log** using **simv-l Lab3.log** and open **vcdplus.vpd .**
7. Select all the signals and open DVE window.
8. Match the result with the table.

**Section 3\_3:**

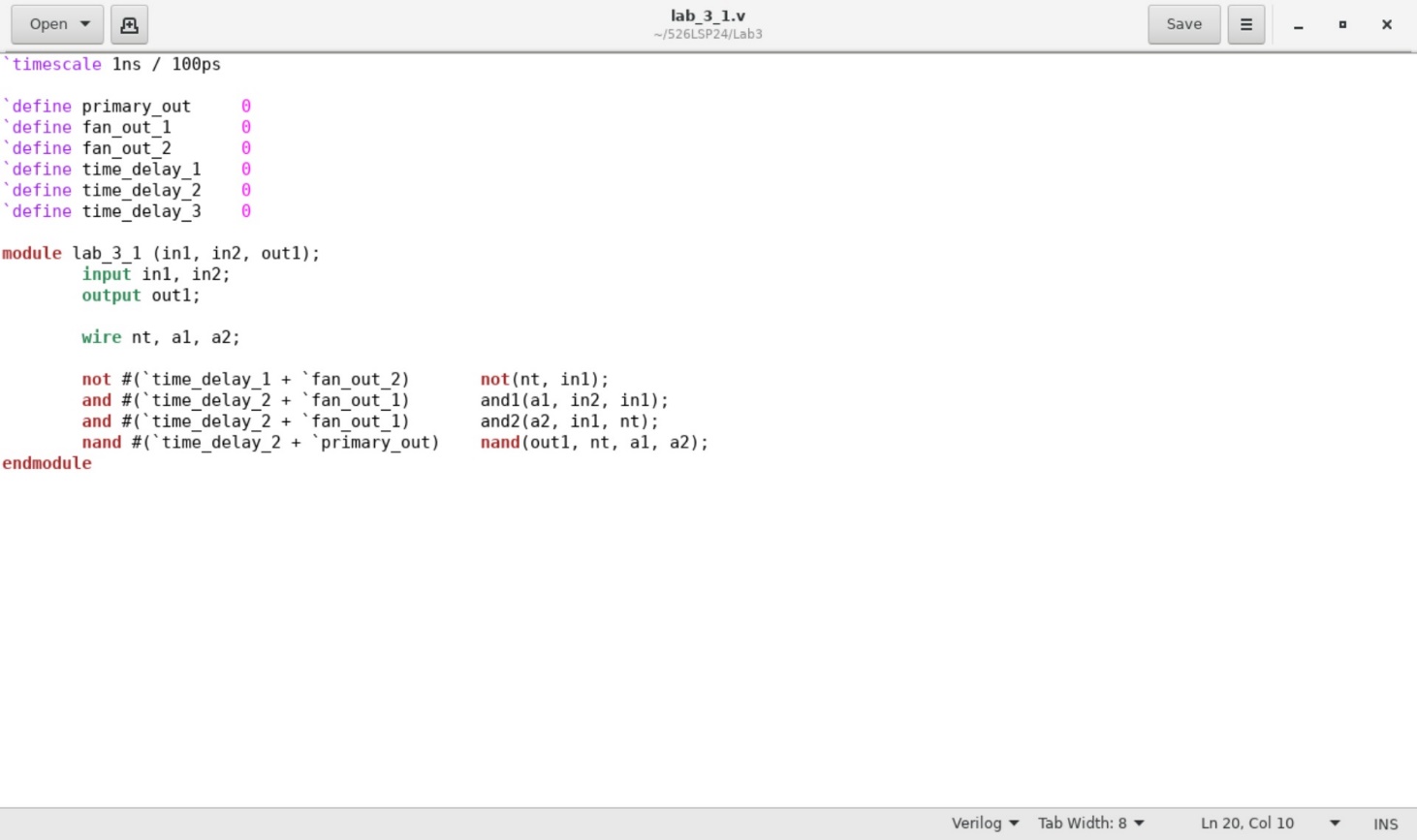
1. Create a new file name as [**Lab3\_3.v**](mailto:Lab_3_@.v) **.**
2. Write the code exactly as in the lab manual and set the delay from the lab manual.
3. Then, create another file name as **Lab3\_3\_tb.v** , write the code as it was with all the possible combinations of the truth table.
4. After that, gave command **vcs -debug\_access+all Lab\_3\_3.v Lab\_3\_3.tb.v** to check the simulations and fix the error.
5. Gave Command **simv** .
6. Create the log file as **Lab\_3\_3.Log** using **simv-l Lab3.log** and open **vcdplus.vpd .**
7. Select all the signals and open DVE window.
8. Match the result with the table.

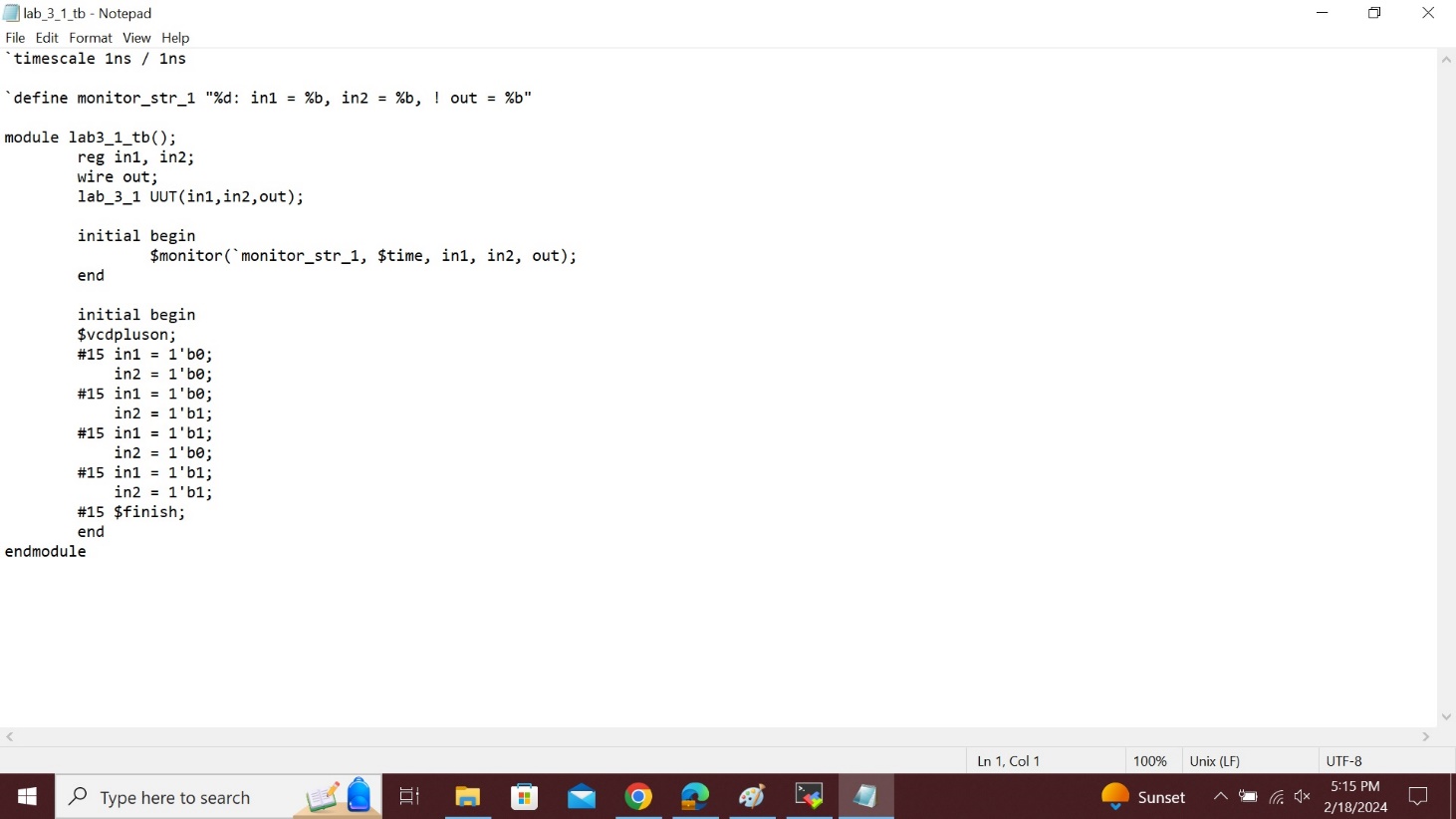
**Discussion:**

The experiment's findings showed that changing the delay settings significantly affected how the rudimentary circuit behaved. The overall speed and dependability of the circuit were impacted by delays in signal propagation that occurred when delays were raised above specific thresholds. On the other hand, lowering delays below ideal thresholds may lead to irregular behavior and timing infractions.

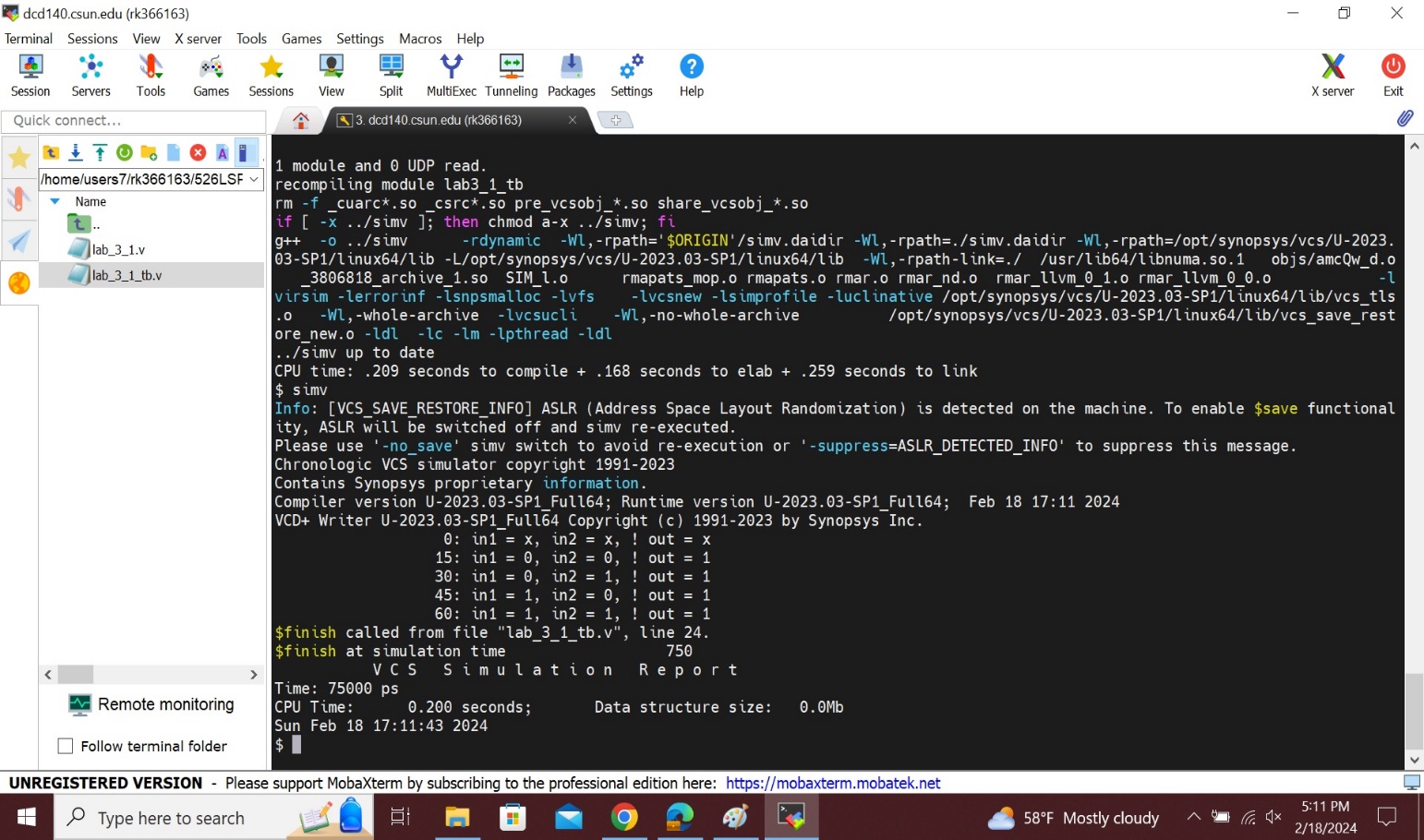
**Section-1**

**Code 3\_1:**

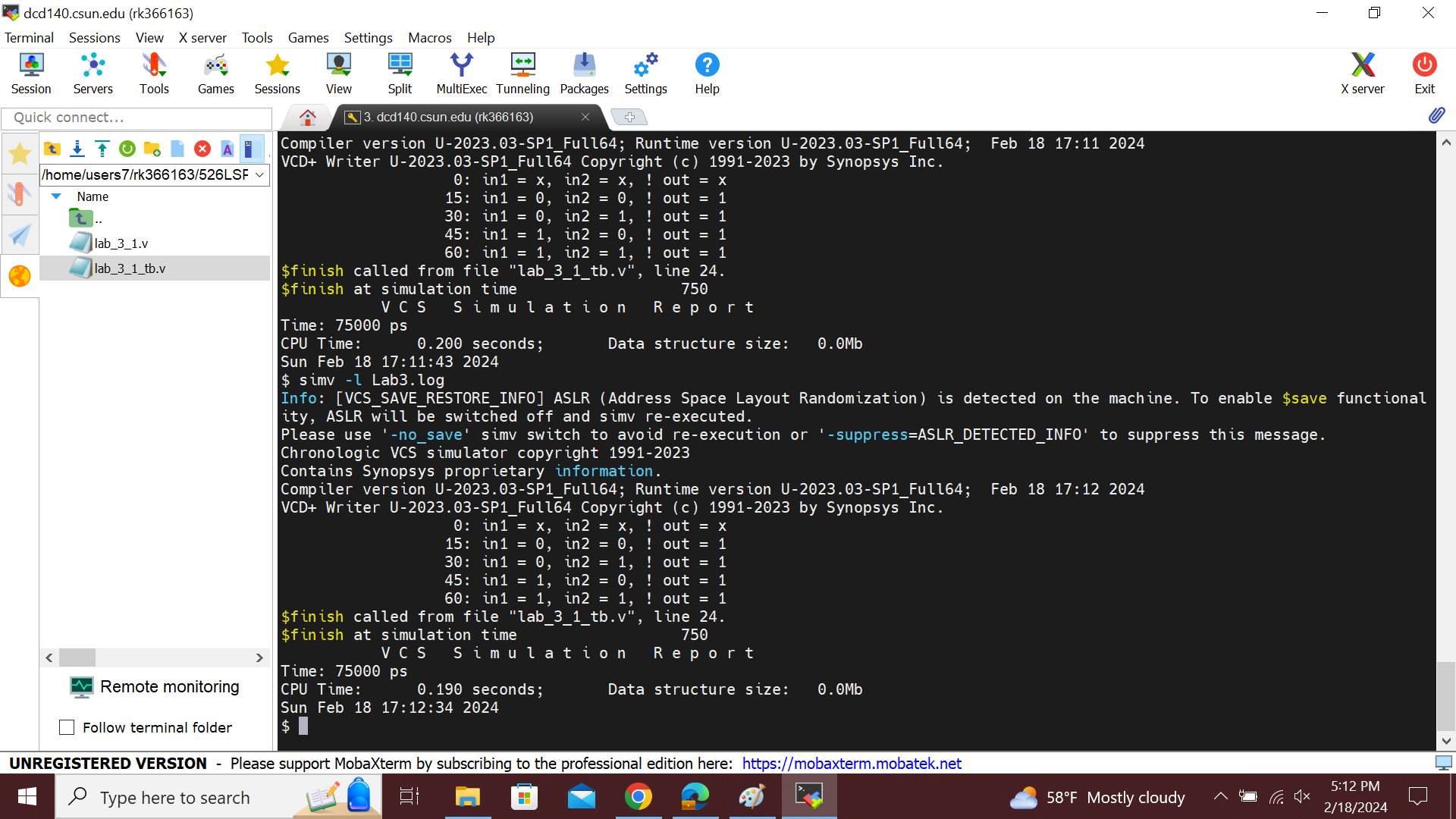




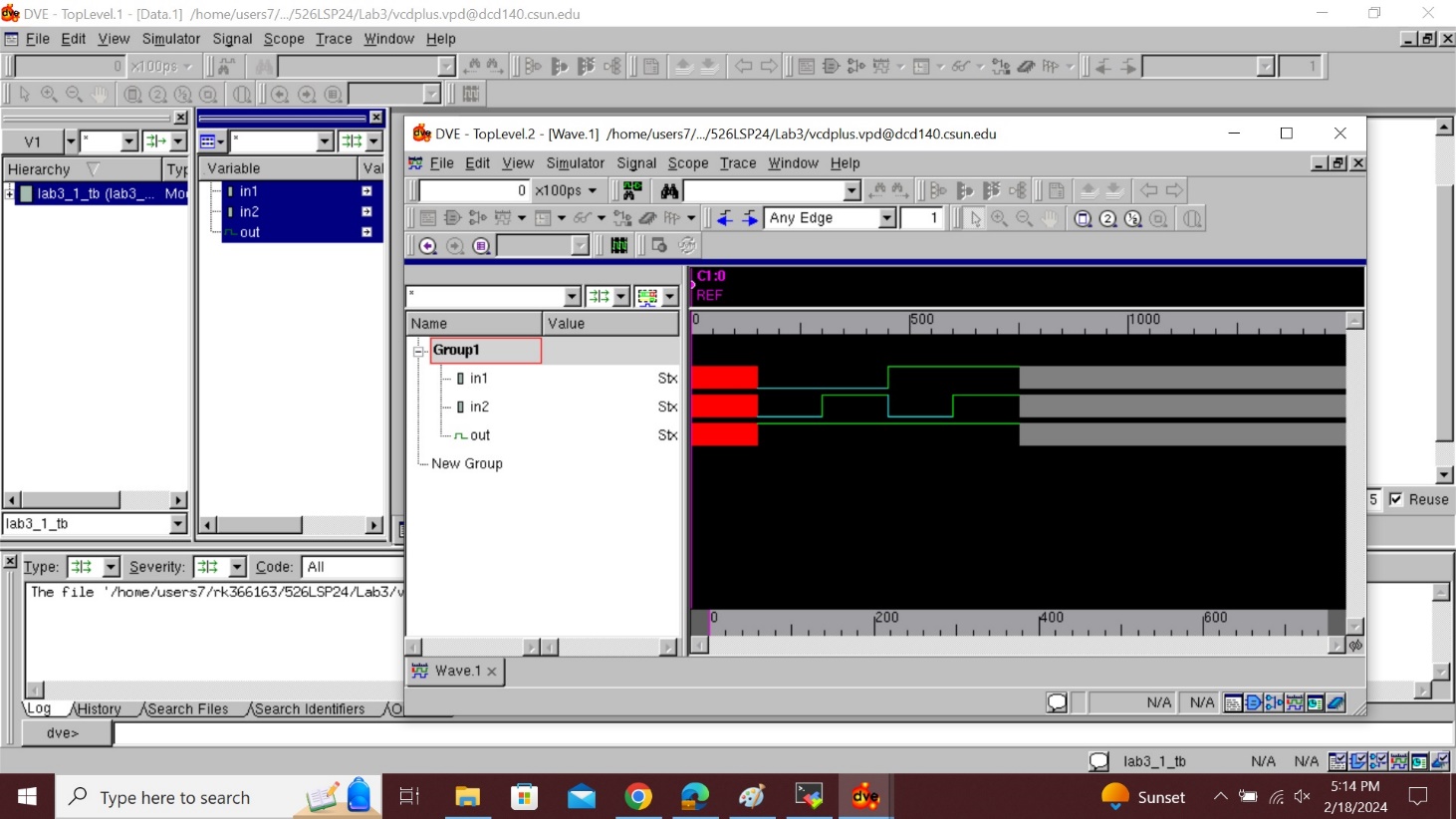
**Simv 3\_1:**



**Log file 3\_1:**

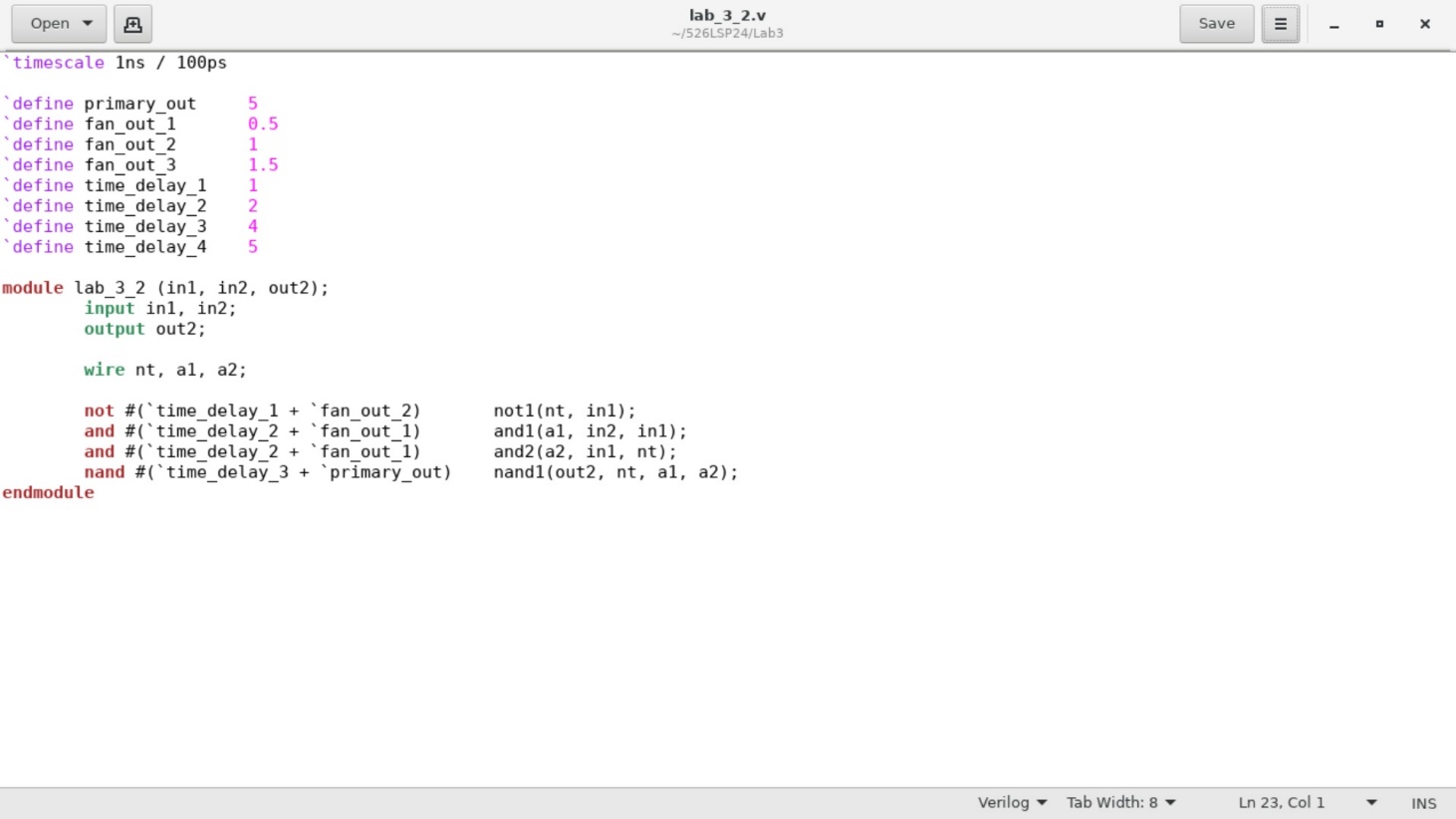


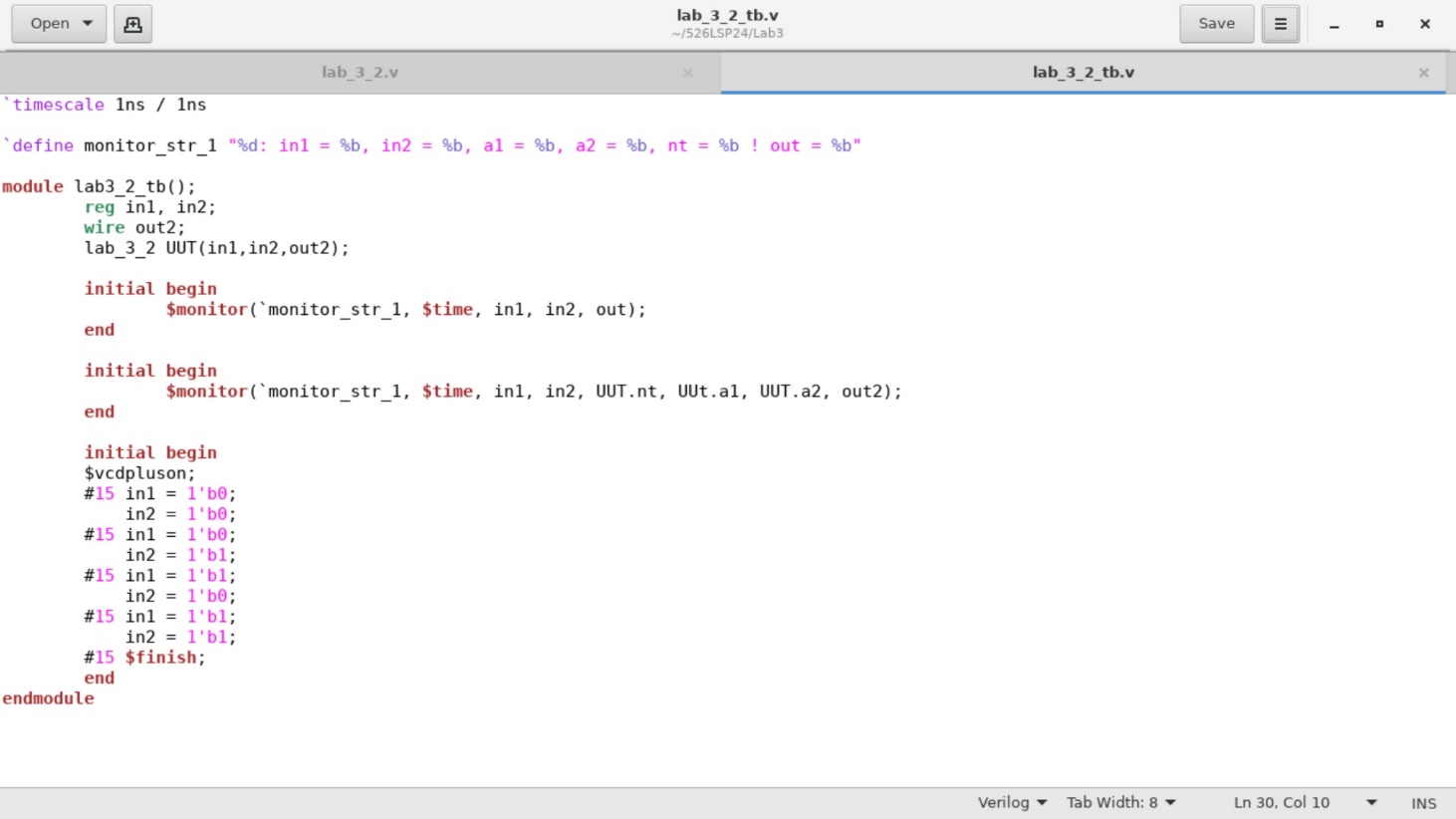
**Wave 3\_1:**



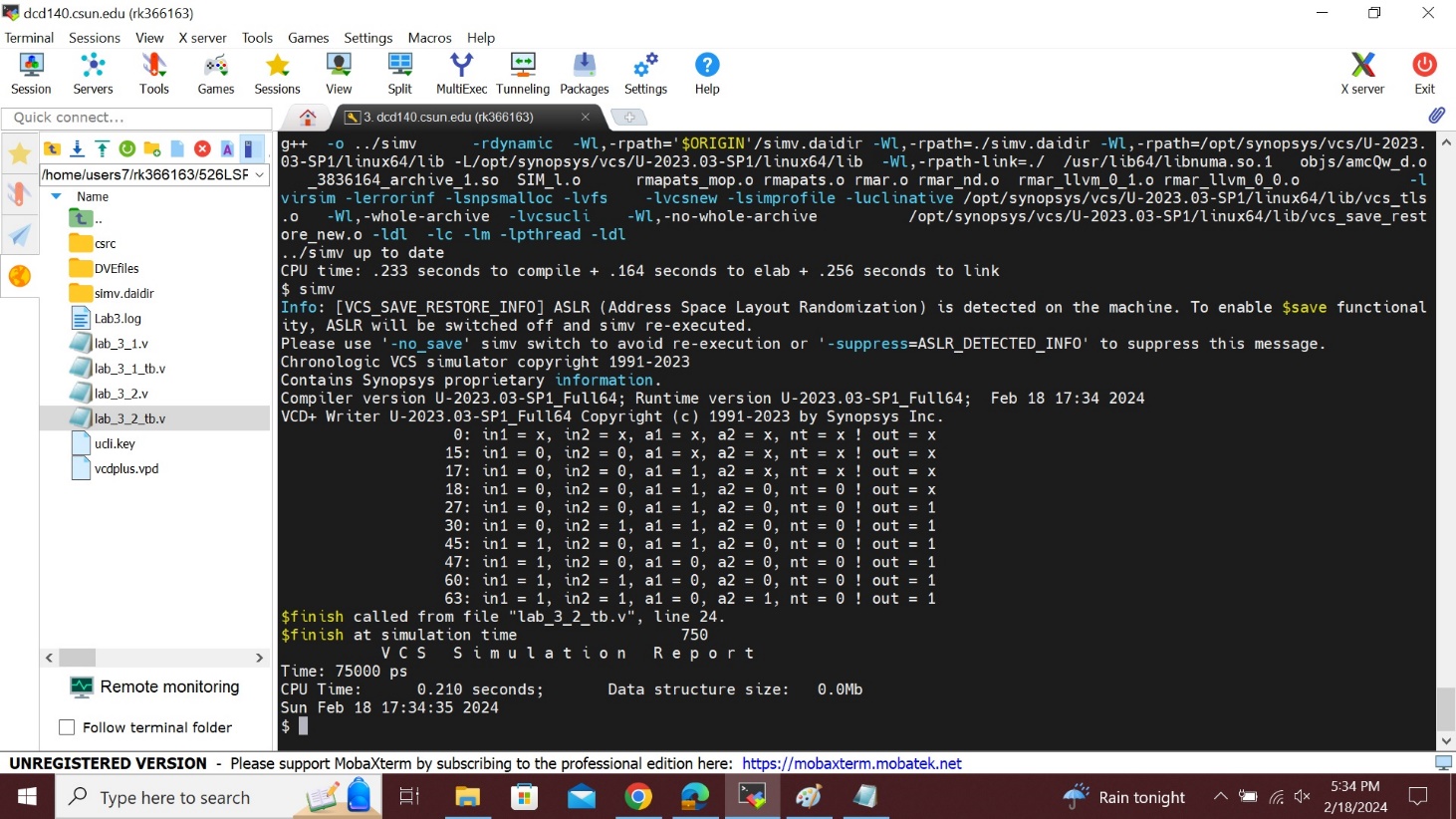
**Section-2**

**Code 3\_2:**

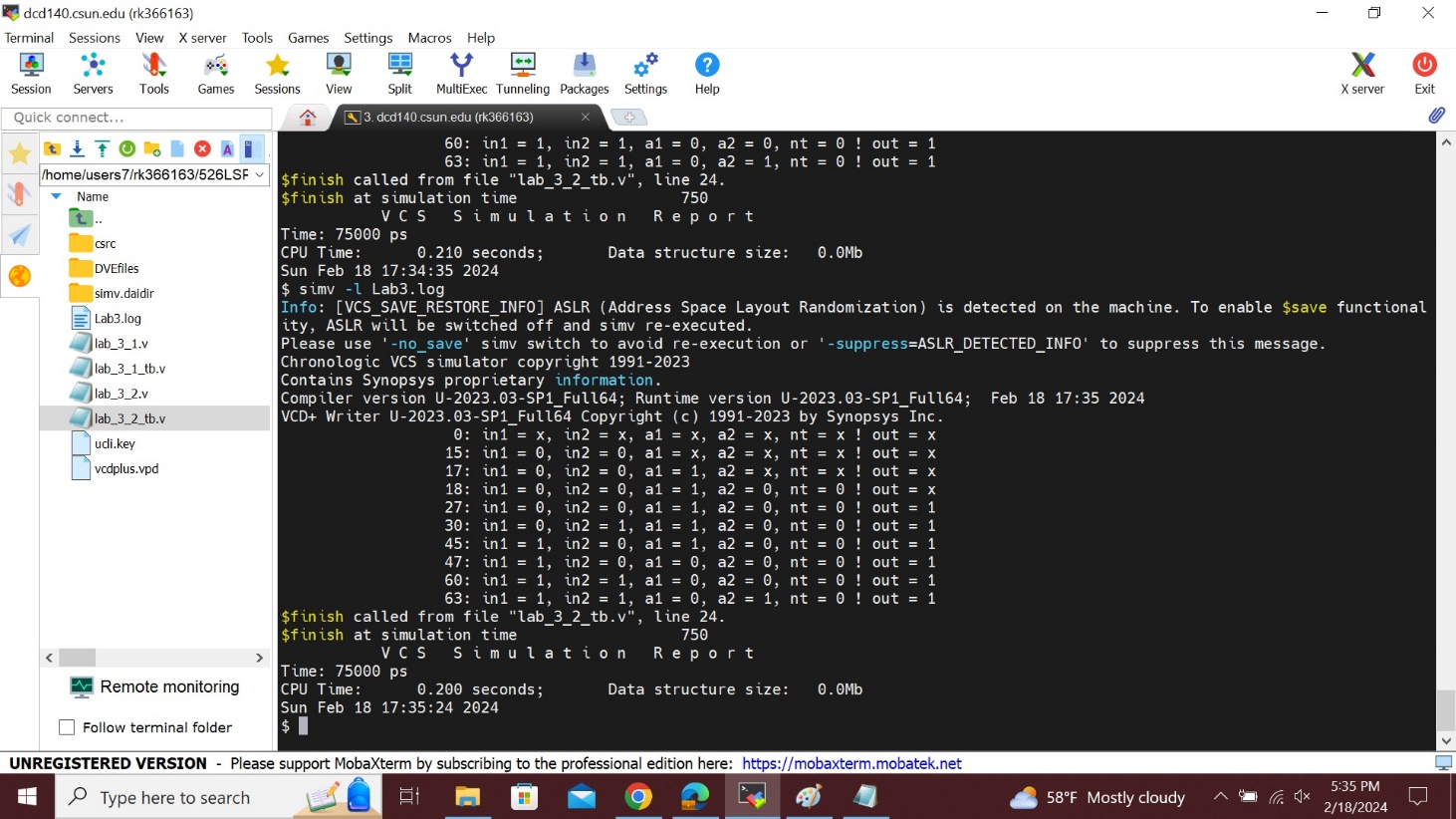




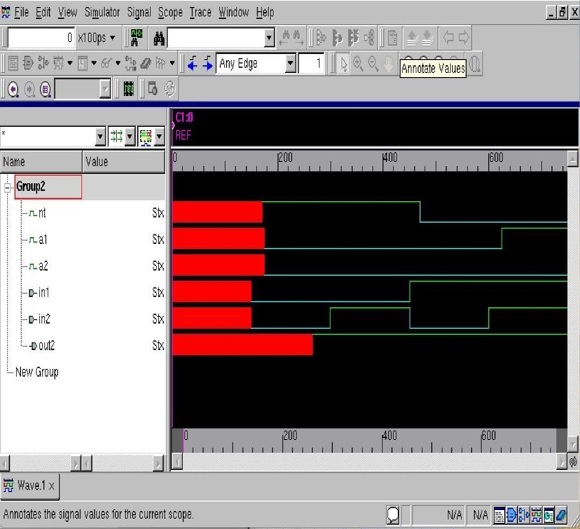
**Simv 3\_2:**



**Log File 3\_2:**

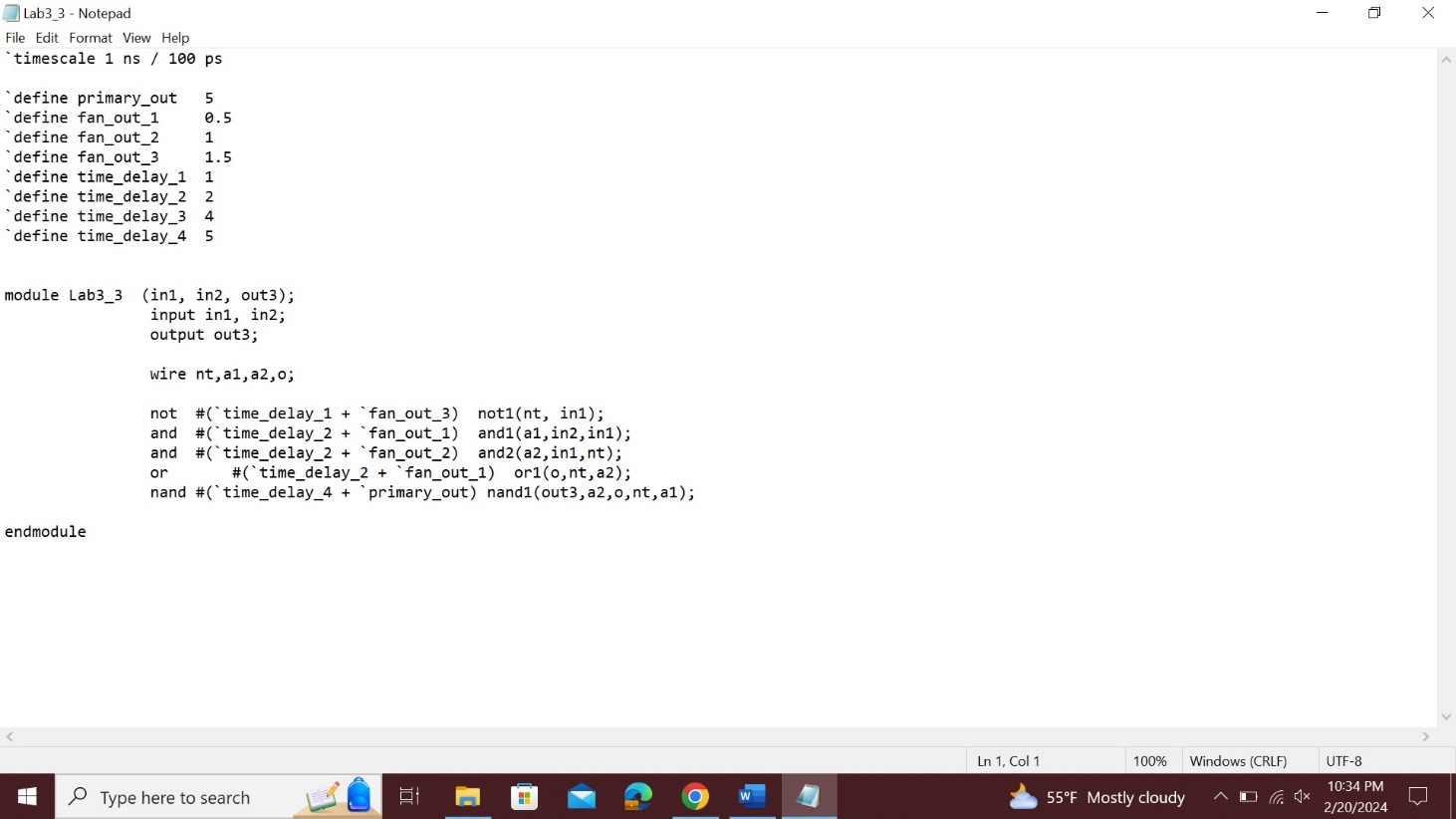


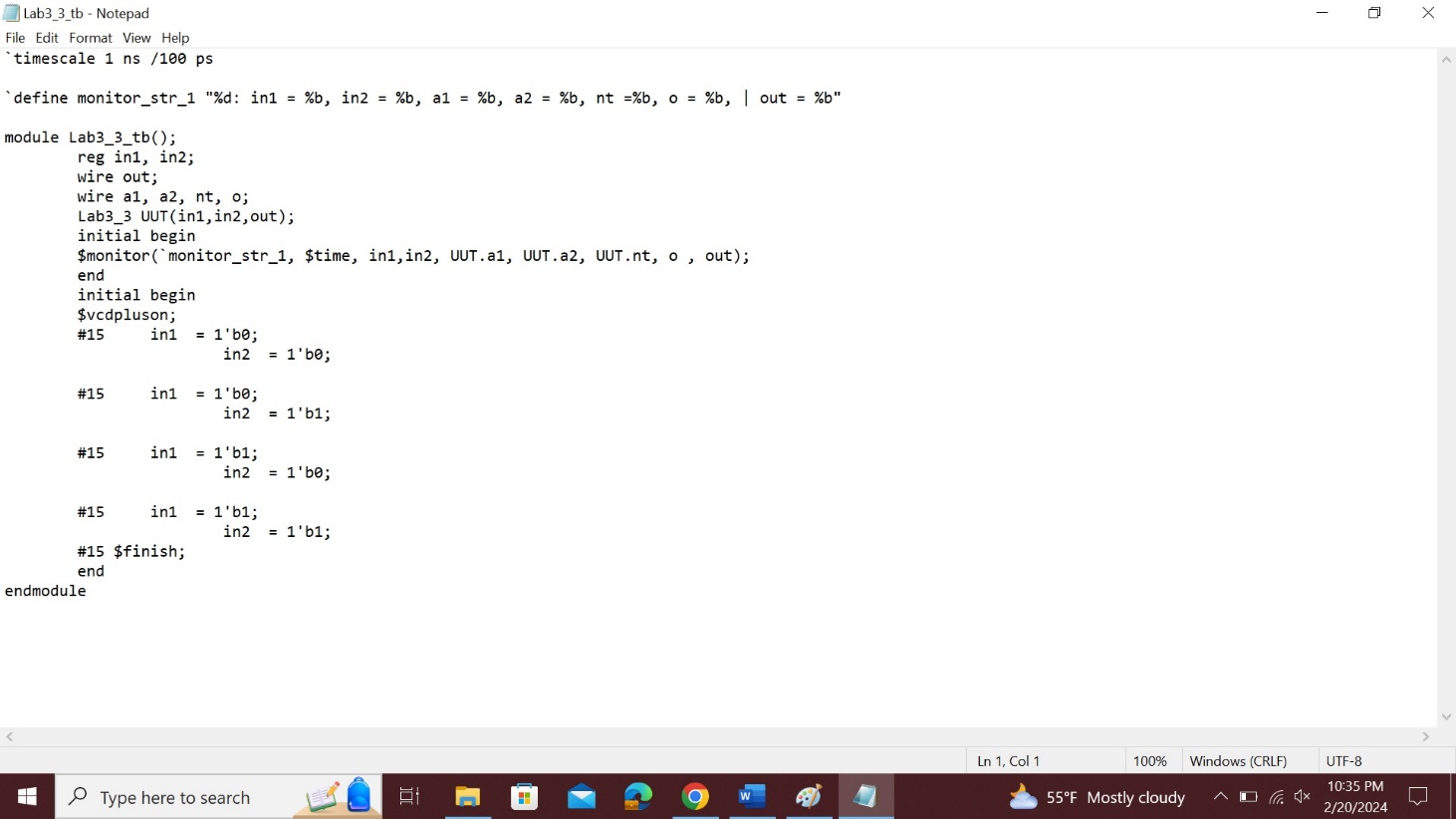
**Wave 3\_2:**



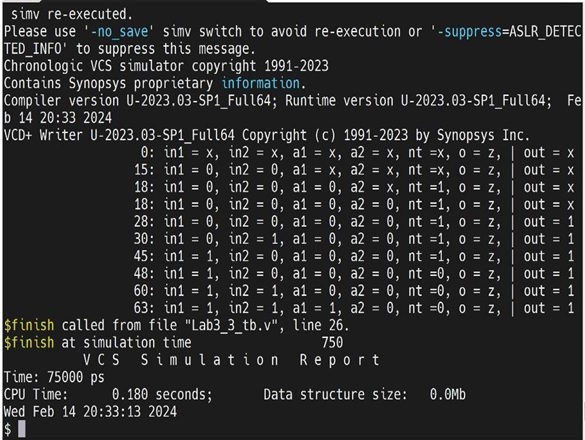
**Section-3**

**Code 3\_3:**

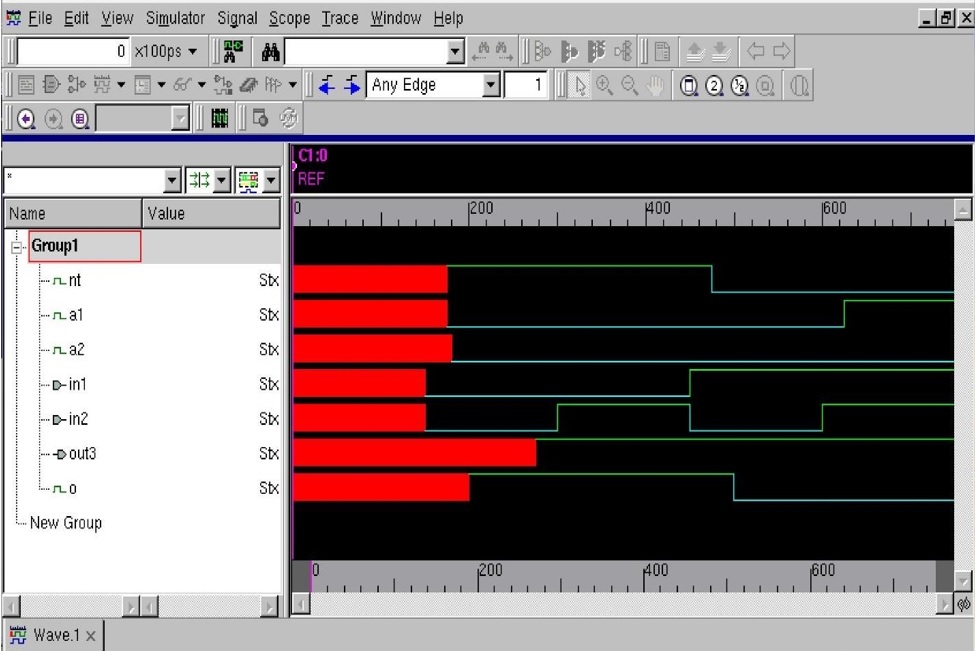




**Simv 3\_2:**

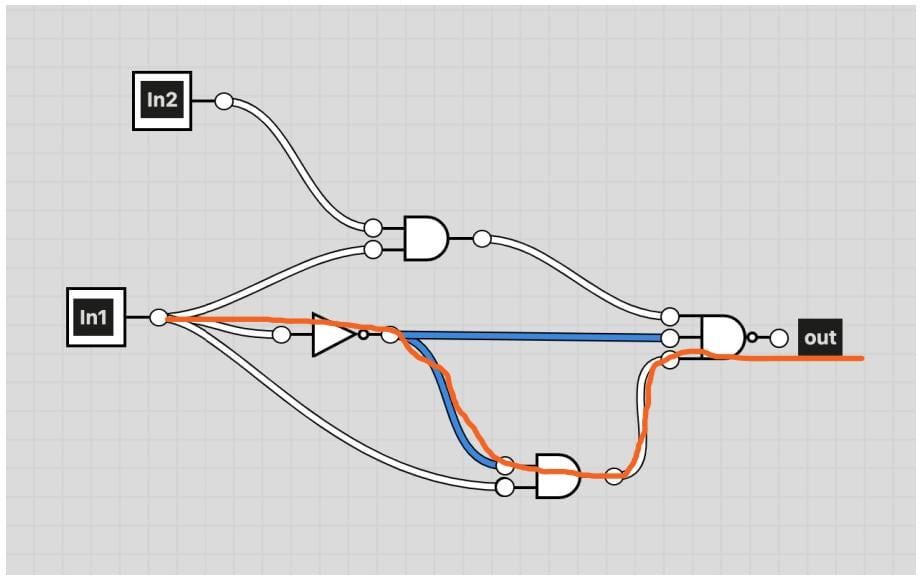


**Wave 3\_3:**



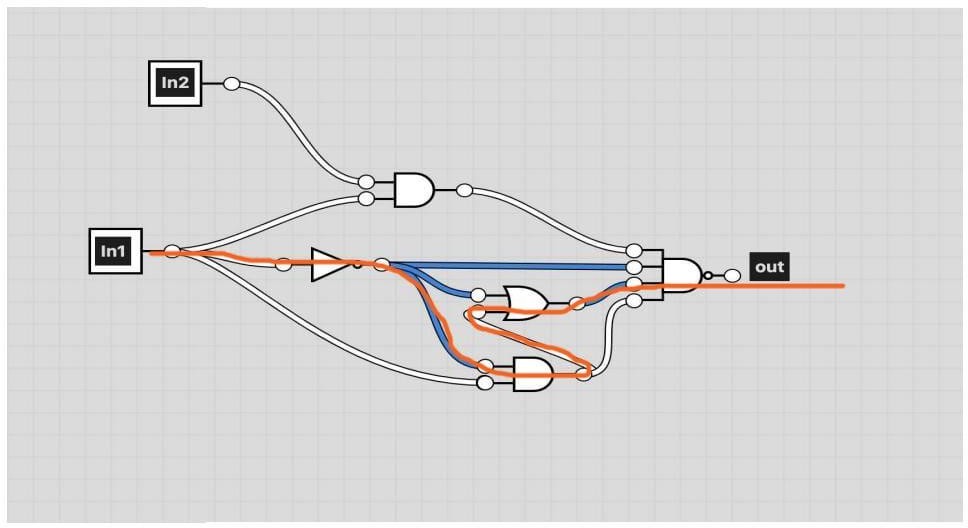
**Lab report questions:**

1. **What is the longest path of the 1st circuit?**



In the above figure, I have drawn the longest path of the circuit that is input which travels from the NOT gate first and then travels to the AND gates, which reaches the final output through the NAND gate. comparing two remaining two paths this is the longest path because other path has only two gates to reach the output where as in this path it has to travel in 3 gates which makes delay in time.

1. **What is the longest path of the 2nd circuit?**



The longest path of the circuit is drawn above is because the input starts from the NOT gate and it travels to the AND gate, then it goes to the OR gate and finally the output comes out through the NAND gate.

On comparing to all other paths, this is the longest part because it has to travel through 4 gates.

# **Analysis of result:**

# Primitive delays are the shortest time delays that can happen when a signal goes through a gate or group of gates in a digital circuit. A basic delay element in digital circuits is produced by this gate combination. The exact delay period will vary based on the circuit's gate characteristics and gate propagation delays. In this lab 1st initial the delays are zero and in second part when we change the values of primitives then the delay will be changed. Finally, the output will be say that the propagation delay will be there for the different delays for their individual values what we given in the code.

**Conclusion:**

In this lab, we completed the gate delays for the given primitives and the numeric values by using some commands and some tools by the linux synopsis VCS.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, neither have I allowed nor I will let anyone to copy my work.

Name(printed) Raj Kumar

Name(signed) Raj Kumar

Date 02/18/2024